IN THE TITLE

Please amend the Title as follows:

~~METHODS AND~~ APPARATUS FOR ADAPTIVELY ADJUSTING A DATA RECEIVER

IN THE SPECIFICATION

Please delete the paragraphs beginning on page 3, line 25, starting with and including the heading, Summary of the Invention, through page 5, line 7, before the heading Brief Description of the Drawings.

Please insert the following paragraphs beginning on page 6, line 21 before the current paragraph beginning on page 6, line 21:

In an embodiment, an electronic device includes a data corrector that provides adjustment information for adjusting the trip point of data receivers included in the electronic device. For offsets in the trip point from a reference voltage, VREF, the data corrector provides adjustment signals that shift the trip point of the data receivers in the electronic device relative to VREF. The data corrector uses differential clock signals, and VREF to generate the set of adjustment signals.

In another embodiment of the present invention, a data receiver includes a receiver having a trip point, and a trip point adjustor. The trip point adjustor uses received adjustment vectors to provide signals to the receiver for adjusting the receiver's trip point.

In another embodiment of the present invention, a data corrector includes a pair of ancillary data receivers and a corrector controller that provides the ancillary data receivers with adjustment vectors. The corrector controller also supplies adjustment vectors to data receivers external to the data corrector. A voltage reference, VREF, is coupled to the ancillary data receivers, along with coupling differential clock signals at the data ports to the ancillary data receivers. The output signals of the ancillary data receivers are compared by a phase detector to determine if they cross concurrently at a zero point for a signal transition (high to low or low to high). If these output signals do not cross concurrently, adjustment vectors are generated and coupled to the ancillary data receivers to adjust their trip point relative to (VCC/2). Adjustment vectors are continually supplied to the two ancillary data receivers, adjusting their trip point until their output signals cross concurrently. The adjustment vectors that result in the output signals from the ancillary data receivers crossing concurrently are selected as the adjustment vectors that the corrector controller supplies to data receivers external to the data corrector.

In another embodiment of the present invention, a phase detector includes circuitry for balancing two signals and comparing a zero crossing of the two signals. The phase detector compares the rising edge of one clock signal with the falling edge of the other clock signal.

In another embodiment of the present invention, a processing system includes a central processing unit, and a plurality of memory devices having a data corrector for supplying adjustment vectors to the data receivers included in each memory device. The memory device receives differential system clocks, and a voltage reference, VREF, to generate the adjustment vectors for the data receivers in the memory devices.

In another embodiment of the present invention, a method of operating a data corrector includes providing two clock signals to a pair of ancillary data receivers, determining a difference between the output signals of the ancillary data receivers, and generating adjustment vectors correlated to the difference in the output signals of the ancillary data receivers. One clock signal is coupled to the data port of one ancillary data receiver, and the other clock signal is coupled to the data port of the other ancillary data receiver.